CLAIMS

1. A template formed from a layered structure comprising a substrate and a single-phase polymer layer positioned on the substrate, wherein the polymer layer comprises a textured surface, the texturing being caused by induction of stress in the polymer layer.

2. A template according to claim 1, additionally comprising a semiconductor layer positioned on the polymer layer.

3. A template according to claim 1 or claim 2, wherein the single-phase polymer is selected from polymethylglutarimide (PMGI), polymethylmethacrylate (PMMA) and photoresist AZ5214E.

4. A template according to claim 2 or claim 3, wherein the semiconductor is germanium.

5. A template according to any preceding claim, wherein the substrate comprises silicon.

6. A template according to any preceding claim, wherein the textured surface comprises parallel grooves.

7. A template according to any preceding claim, wherein the thickness of the single-phase polymer layer is 50-300 nm.

8. A template according to any of claims 2 to 6, wherein the thickness of the semiconductor layer is approximately 10 nm.

9. A method of manufacture of a structure on the nanometre scale comprising the steps of:

providing a template as defined in any of claims 1 to 8;

molding a material on to the template; and

removing the molded material from the template to provide a structure on the nanometre scale.

10. A method according to claim 9, wherein the structure is an array, a grid, an optical device or an electronic device.

11. A method according to claim 10, wherein the optical

device is a polariser.

12. A method according to claim 10, wherein the array is a magnetic wire array.

13. A method according to claim 12, wherein the magnetic wire array comprises Permalloy.

14. A method of making a template comprising the steps of:

depositing a layer of a single-phase polymer on to a substrate;

baking the resulting structure from the deposition step at a temperature below the glass transition temperature (T_g) of the single-phase polymer;

texturing a surface of the polymer layer by inducing stress in the polymer layer; and

annealing the resulting structure from the stress-induction step to provide a template.

15. A method according to claim 14 additionally comprising the step of depositing a semiconductor layer on to the polymer layer.

16. A method according to claim 14 or claim 15, wherein the temperature employed in the baking step is in the range 120-200 °C.

17. A method according to any of claims 14 to 16, wherein the stress induced in the polymer is in the range 0.5-1 MPa.

18. A method according to any of claims 14 to 17, wherein stress is induced in the polymer layer using a load bearing member comprising at least one contact surface engaging the surface to be textured.

19. A method according to claim 18, wherein the load bearing member comprises polydimethylsiloxane (PDMS).

20. A method according to claim 18 or claim 19, wherein the contact surface of the load bearing member is textured.

21. A method according to any of claims 14 to 20, wherein the single-phase polymer is selected from PMGI, PMMA and photoresist AZ5214E.

22. A method according to any of claims 15 to 21 wherein the semiconductor is germanium.

23. A method according to any of claims 14 to 22, wherein the substrate comprises silicon.

24. A method according to any of claims 14 to 23, wherein stress-induction in the polymer layer results in the formation of parallel grooves in the surface of the polymer layer.

25. A method according to any of claims 14 to 24, wherein the thickness of the polymer layer is 50-300 nm.

26. A method according to any of claims 15 to 25, wherein the thickness of the semiconductor layer is approximately 10 nm.